Preetham SK

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Education

- **Vellore Institute of Technology** — Chennai, India
  B.Tech in Electrical and Electronics Engineering — *September 2022 – May 2026*
  - **CGPA**: 9.18 / 10 (German Grade Equivalent: 1.4) | Class Rank: 14 / 220
  - **Relevant Coursework**: Digital Electronics, Electronic Devices and Circuits, Analog Electronics, Electromagnetic Theory, Signals and Systems, Digital Signal Processing, Control Systems, Complex Variables and Linear Algebra, Differential Equations and Transforms, Probability and Statistics, Computer Programming: Java
  - **Language Training**: German I (Grade A) – formal university-level German language course

- **Senthil Public School** — Salem, India
  Class XII, CBSE – 85.0% — *2022*

- **Sri Swamy International School** — Salem, India
  Class X, CBSE – 93.0% — *2020*

Publications

[1] **Patent [Published]** – Dynamic Reconfigurable Binary Multiplier System and Method Thereof. [GitHub]
Indian Patent Application No. 202541080342 | Published: 19 September 2025
Contribution: Designed reconfigurable binary multiplier using quadrant decomposition and adaptive row bypassing in Verilog HDL; complete RTL-to-GDSII using Cadence Genus and Innovus across TSMC 180nm and 90nm.
Inventors: Dr. S. Umadevi, **Preetham SK**, Nakul S, Sumit Kumar

[2] **Patent [Under Review]** – Low-Power High-Performance Fixed-Point Softmax Processing Unit with LUT-Based Exponent and Mitchell Logarithmic Divider. [GitHub]
Contribution: Designed fixed-point Softmax architecture with dual-mode LUT exponent block and 8-stage pipelined Mitchell divider; 100 MHz on TSMC 180nm, 97.89% MNIST accuracy, 8.9× throughput improvement.
Inventors: **Preetham SK**, Sreehari R, Dr. P. Sasipriya, Dr. A. Anita Angeline, Prof. V. Anantha Krishnan

[3] **SCI Journal [Under Review]** – Adaptive Quadrant Multiplier with Dynamic Reconfigurable Structure. [GitHub]
Contribution: Developed RCA-based Adaptive Quadrant multiplier with row bypassing; at 90nm achieves 98.92% lower power, 28.19% smaller area, 98.47% improved PDP; validated using Cadence Genus and Innovus.
Authors: Adhiyamaan, **Preetham SK**, Dr. S. Umadevi, Ms. Rekha

[4] **Book Chapter [Accepted]** – FPGA Based Solar Powered EV Charging Station: Smart Infrastructure for a Sustainable Future. [GitHub]
Smart Technologies for Smart Buildings | CRC Press, Taylor & Francis Group | ISBN: 9781041093626
Contribution: Designed 11-state FSM-based charge controller and P&O MPPT algorithm in Verilog HDL; managed charge states, fault detection, and power routing; verified using ModelSim.
Authors: Nakul S, **Preetham SK**, Pradeesh R, Kartheesan K, Dr. O.V. Gnana Swathika

[5] **Research Article [Under Review]** – Convolutional Neural Networks on Dedicated Hardware: A Comprehensive Survey of VLSI, FPGA and ASIC Implementations Across Real World Application Domains. [GitHub]
Contribution: Cross-domain survey of CNN accelerators across FPGA, ASIC, and VLSI platforms; benchmarks include 587.52 GOPs at 142.95 GOPs/W and 1.145 TFLOP/s at 34.9 µW.
Authors: **Preetham SK**, Dr. Lavanya V, Dr. Meera P S

[6] **SCI Journal [Work In Progress]** – Silicon-Level Implementation and Performance Characterisation of a Fixed-Point Softmax Processing Unit for DNN Inference Accelerators. [GitHub]
Contribution: Completed RTL-to-GDSII on TSMC 180nm using Cadence Innovus; Single-LUT: 5152 cells, 13.44 mW; Dual-LUT: 5026 cells, 12.14 mW; both at 100 MHz with full physical sign-off.
Authors: **Preetham SK**, Sreehari R, Dr. P. Sasipriya, Dr. A. Anita Angeline, Prof. V. Anantha Krishnan

Internship Experience

- **Center for Nano Electronics and VLSI Design (CNVD), VIT Chennai** — Chennai, India
  Summer Research Intern – Guide: Dr. S. Umadevi — *3 June 2024 – 10 August 2024*
  - **MAC Unit & Synthesis**: Designed a 16×16 MAC unit in Verilog HDL using Row Bypass Adder scheme; functionally verified using Cadence® NC Launch; gate-level synthesis using Cadence® Genus. Architecture inspired Indian Patent No. 202541080342 (published September 2025).

- **Centre for Smart Grid Technologies (CSGT), VIT Chennai** — Chennai, India
  Summer Research Intern – Guide: Dr. O.V. Gnana Swathika — *1 May 2025 – 31 July 2025*
  - **Finite State Machine & Maximum Power Point Tracking**: Designed an 11-state FSM-based EV charging controller and P&O MPPT algorithm in Verilog HDL; verified using ModelSim. Contributed to accepted book chapter – *Smart Technologies for Smart Buildings*, CRC Press (ISBN: 9781041093626).

- **Maven Silicon** Online
  VLSI Physical Design Intern – Ref: MS/B2BPDI/2025-26-135 *16 May 2025 – 04 July 2025*
  - **PD Flow**: Complete RTL-to-GDSII physical design for SPI controller using Qflow on OSU 0.18µm – synthesis (Yosys/ABC), placement (Graywolf), routing (Qrouter), STA (Vesta); DRC/LVS clean, fabrication-ready GDSII generated.
- **SkillDzire (AICTE - All India Council for Technical Education, Recognized)** Online
  VLSI Design Intern *5 May 2025 – 20 June 2025*
  - **RTL Design**: Designed and verified 5 FSM-based Verilog RTL modules – UART, synchronous FIFO, Traffic Light Controller, Temperature Controller, and Washing Machine Controller using ModelSim.

Projects

- **Digital VLSI SoC Design & Planning** (Verilog, OpenLANE, Sky130 PDK, Magic VLSI) [GitHub]
  - Complete RTL-to-GDSII on PicoRV32a RISC-V – synthesis, floorplan, placement, CTS, routing, STA; custom cell `sky130_vsdinv` designed and integrated; timing closure via ECO; DRC/LVS clean; 17108 cells, 40.44 MHz, fabrication-ready GDSII.
- **RISC-V CPU Design using TL-Verilog** (TL-Verilog, Makerchip) [GitHub]
  - 5-stage pipelined RISC-V RV32I core – fetch, decode, execute, memory, writeback; data hazard bypassing, branch control logic; verified on Makerchip.
- **VLSI Design Automation Using TCL – VSDSYNTH** (TCL, Yosys, OpenTimer) [GitHub]
  - CSV-driven RTL-to-QoR automation framework integrating Yosys synthesis and OpenTimer STA; validated on openMSP430 – 6845 gates, 10000 paths analysed, QoR dashboard generated.
- **SPI Controller - Timing Closure and Physical Sign-off** (Qflow, Yosys, Magic, Netgen) [GitHub]
  - RTL-to-GDSII SPI controller on OSU 0.18 µm: 3106 cells, 22,417 routes (0 failures); 4.3 ns delay, 348 ps skew; DRC/LVS clean; fabrication-ready GDSII.
- **RTL Digital Design Modules using Verilog** (Verilog HDL, ModelSim) [GitHub]
  - 5 FSM-based RTL modules – UART, FIFO, Traffic Light Controller, Temperature Controller, Washing Machine Controller; structured testbenches, ModelSim verified.
- **Packaging Design and Simulation using ANSYS** (ANSYS AEDT, Mechanical) [GitHub]
  - Thermal simulation of flip-chip BGA in ANSYS Electronics Desktop; 3D wire bond package cross-section modelling – die, substrate, encapsulation; thermo-mechanical reliability analysis.

Skills Summary

- **Languages:** Verilog HDL, TL-Verilog, TCL, C, Python
- **EDA Tools:** Cadence® NC Launch, Cadence® Genus, Cadence® Innovus, ModelSim, OpenLANE, Yosys, Magic VLSI, Qflow, Graywolf, Qrouter, Netgen, OpenTimer, Vesta, ANSYS AEDT, Makerchip IDE, HSPICE
- **Other Tools:** LT Spice, Eagle CAD, KiCAD, MATLAB/Simulink
- **Platforms:** Linux, Windows, Arduino
- **Spoken Languages:** English (Fluent), Tamil (Native), German (Basic – University Level, Grade A)

Certifications

- **CeNSE Winter School on Semiconductor Technology [Certificate of Distinction]** [Verify] *Dec 2025*
  Centre for Nano Science and Engineering, IISc Bengaluru. Scored above 75%.
- **Chip-based VLSI Design for Industrial Applications [Specialisation]** [Verify] *Sep 2025*
  L&T EduTech via Coursera.
  Certificates: Fundamentals of Digital Design for VLSI Chip Design, VLSI Chip Design and Simulation with Electric VLSI EDA Tool, Design of Digital Circuits with VHDL Programming, FPGA Architecture Based System for Industrial Application
- **RISC-V Processor – RV32I Base ISA** [Verify] *Feb 2025*
  Maven Silicon.

Awards & Achievements

- **Danfoss Innovator Award 2025 [Finalist]** – Selected as finalist for OXALIS DEPPEI (dual-stage air filtration system), Danfoss University Engagement Team, VIT Chennai. *Feb 2025*
- **Robooceana Grand Finale [Certificate of Excellence]** – Selected for Grand Finale of national robotics competition; electronics team member for Raspberry Pi-based hovercraft, IIT Madras Shaastra 2024. *Jan 2024*

Extracurriculars

- **Editor – The Spectrum, Technical Magazine** – Edited and curated technical content for the School of Electrical Engineering annual magazine, VIT Chennai. *2022 – 2025*
- **IEEE Student Chapter** – Volunteer Member, VIT Chennai. *2022 – 2023*
- **VDAT 2024 – 28th International Symposium on VLSI Design and Test** [Verify], VIT Vellore. *Sep 2024*